

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An input buffer receiver comprising:

a buffer input portion for receiving an input signal, said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and a lower supply voltage ~~said large capacitor for~~ providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point ~~approaching~~ is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

2. (Currently Amended) The input buffer receiver of claim 1, wherein the buffer input portion which receives the input signal further comprises:

3 a first transistor of a first conductivity type having a source node to which  
4 the lower supply voltage is applied, a gate node to which a reference  
5 voltage is applied, and a drain node at which the biasing voltage is  
6 developed ;

7 a second transistor of a second conductivity type having a drain node  
8 which is connected to the drain node of the first transistor, and a gate  
9 node at which the biasing voltage is developed, and a source node to  
10 which an upper supply voltage source is applied;

11 a third transistor of the second conductivity type having a drain node  
12 ~~which is connected to the drain of a fourth transistor~~, a gate node at  
13 which the biasing voltage is developed, and a source node to which  
14 the upper supply voltage source is applied;

15 a fourth transistor of the first conductivity type having a source node to  
16 which the lower supply supply voltage is applied, a gate node to  
17 which ~~an~~ the input signal is applied ~~externally~~, and a drain node which  
18 ~~is an input to~~ coupled to the drain of a fourth transistor and to an input  
19 node of the buffer output portion.

1 3. (Previously Presented) The input buffer receiver of claim 2, wherein the  
2 first and fourth transistors are NMOS transistors, and the second and third  
3 transistors are PMOS transistors.

1 4. (Previously Presented) The input buffer receiver of claim 2, wherein the  
2 large capacitor is connected between the sources of the first and fourth  
3 transistors of the buffer input portion and the gate of the second transistor  
4 of the buffer input portion.

1 5. (Previously Presented) The input buffer receiver of claim 2, wherein the  
2 gate of the second transistor is connected to its drain.

1 6. (Previously Presented) The input buffer receiver of claim 2, wherein the  
2 gate of the second transistor is connected to the drain of the first  
3 transistor.

1 7. (Previously Presented) The input buffer receiver of claim 2, wherein the  
2 gate of the second transistor is connected to the gate of the third  
3 transistor.

1 8. (Currently Amended) The input buffer receiver of claim 2, wherein the  
2 buffer output portion which produces the output signal comprises: a first  
3 inverter connected to the drain of the third transistor and the drain of the  
4 ~~fourth transistor;~~ transistor.

9. (Currently Amended) The input buffer receiver of claim 2, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

10. (Previously Presented) The input buffer receiver of claim 1, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{C_p + CHC} \approx 1$$

where:

**CHC** is the capacitance value of the large capacitor,  
and

**C<sub>p</sub>** is the capacitance value of the parasitic capacitor.

11. (Currently Amended) The input buffer receiver of claim 1, wherein the capacitance value of the large capacitor ~~relative to~~ is chosen to be very large with respect to a capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

12. (Currently Amended) An integrated circuit formed on a substrate

comprising:

an input buffer receiver for receiving an input signal ~~and connected to said~~  
~~distribution network~~, said input buffer comprising:

a buffer input portion for receiving the input signal,

said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and

a lower supply voltage, ~~said large capacitor for~~

providing a coupling ratio between said large

capacitor and a parasitic capacitor coupled

between said bias node and a ground reference

point ~~approaching~~ is approximately equal to a

unity value such that a biasing voltage at said

biasing node follows said lower supply voltage to

minimize effects of a ground noise signal between

the lower supply voltage and the ground reference

point ; and

a buffer output portion in communication with the

buffer input portion for producing an output signal.

13. (Currently Amended) The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node ~~which is connected to the drain of a fourth transistor~~, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which an input signal is applied ~~externally~~, and a drain node which is an input to connected to the drain of a fourth transistor and to an input node of the buffer output portion.

1 14. (Previously Presented) The integrated circuit of claim 13, wherein the first  
2 and fourth transistors are NMOS transistors, and the second and third  
3 transistors are PMOS transistors.

1 15. (Previously Presented) The integrated circuit of claim 13, wherein the  
2 large capacitor is connected between the sources of the first and fourth  
3 transistors of the buffer input portion and the gate of the second transistor  
4 of the buffer input portion.

1 16. (Previously Presented) The integrated circuit of claim 13, wherein the gate  
2 of the second transistor is connected to its drain.

1 17. (Previously Presented) The integrated circuit of claim 13, wherein the gate  
2 of the second transistor is connected to the drain of the first transistor.

1 18. (Previously Presented) The integrated circuit of claim 13, wherein the gate  
2 of the second transistor is connected to the gate of the third transistor.

1 19. (Currently Amended) The integrated circuit of claim 13, wherein the buffer  
2 output portion which produces said output signal comprises: a first inverter  
3 connected to the drain of the third transistor and the drain of the fourth  
4 ~~transistor;~~ transistor.

20. (Currently Amended) The integrated circuit of claim 13, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

21. (Previously Presented) The integrated circuit of claim 12, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{C_p + CHC} \approx 1$$

where:

**CHC** is the capacitance value of the large capacitor,  
and

**C<sub>p</sub>** is the capacitance value of the parasitic capacitor.

22. (Currently Amended) The integrated circuit of claim 12, wherein the capacitance value of the large capacitor ~~relative to~~ is chosen to be very large with respect to a capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.



23. (Currently Amended) A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting ~~said~~ a lower supply voltage to said buffer input portion;

forming a large capacitor coupled between the bias node and the lower

supply voltage ~~said large capacitor~~ for providing a coupling ratio

between said large capacitor and a parasitic capacitor coupled

between said bias node and a ground reference point ~~approaching is~~

approximately equal to a unity value such that a biasing voltage at said

biasing node follows said lower supply voltage to minimize effects of

**[[a]]** said ground noise signal ~~between the lower supply voltage and~~

the ground reference point; and

forming a buffer output portion on said substrate in communication with

the buffer input portion for producing an output signal.

24. (Currently Amended) The method of claim 23, wherein forming the buffer input portion further comprises the steps of:

forming a first transistor of a first conductivity type on said substrate;

4           applying the lower supply voltage to a source node of the first transistor;

5           applying a reference voltage to a gate node of the first transistor;

6           connecting a drain node of the first transistor to develop ~~[[as]]~~ a biasing  
7           voltage at said drain node;

8           forming a second transistor of a second conductivity type on said  
9           substrate;

10          connecting a drain node of the second transistor to the drain node of the  
11          first transistor;

12          connecting a gate node of the second transistor to the drain node of the  
13          first transistor for developing the biasing voltage; and

14          connecting a source node of the second transistor to an upper supply  
15          voltage;

16          forming a third transistor of the second conductivity type on said substrate;

17          ~~connecting a drain node of the third transistor to the drain of a fourth~~  
18          ~~transistor;~~

19          connecting a gate node of the third transistor to the drain node of the first  
20          transistor for developing the biasing voltage;

21 connecting a source node of the third transistor to the upper supply  
22 voltage source;  
  
23 forming a fourth transistor of the first conductivity type on said substrate;  
  
24 connecting a source node of the fourth transistor to the lower supply  
25 voltage;  
  
26 connecting a gate node of the fourth transistor to receive an input signal  
27 externally; and  
  
28 connecting a drain node of the fourth transistor to an input to a drain node  
29 of the third transistor and to an input node of the buffer output portion.

1 25. (Previously Presented) The method of claim 24, wherein the first and  
2 fourth transistors are NMOS transistors, and the second and third  
3 transistors are PMOS transistors.

1 26. (Previously Presented) The method of claim 24, wherein forming the large  
2 capacitor comprises the step of:  
  
3 connecting said large capacitor between the sources of the first and fourth  
4 transistors of the buffer input portion and the gate of the second  
5 transistor of the buffer input portion.

1 27. (Previously Presented) The method of claim 24, wherein forming the  
2 buffer input portion further comprises the steps of:

3 connecting the gate of the second transistor to its drain.

1 28. (Previously Presented) The method of claim 24, wherein forming the  
2 buffer input portion further comprises the steps of:

3 connecting the gate of the second transistor to the gate of the third  
4 transistor.

1 29. (Currently Amended) The method of claim 24, wherein forming the buffer  
2 output portion which ~~produces output~~ produces the output signal  
3 comprises the step of:

4 forming a first inverter on said substrate; and

5 connecting an input of said first inverter to the drain of the third transistor  
6 and the drain of the fourth ~~transistor;~~ transistor.

1 30. (Currently Amended) The method of claim 24, wherein the third transistor  
2 and the fourth transistor activate and deactivate almost simultaneously as  
3 determined by said input signal to minimize the effects of ground noise on  
4 a delay jitter factor of said input buffer.

31. (Previously Presented) The method of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{C_p + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor,  
and

C<sub>p</sub> is the capacitance value of the parasitic capacitor.

32. (Currently Amended) The method of claim 23, wherein the capacitance value of the large capacitor ~~relative to~~ is chosen to be very large with respect to a capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.

33. (Currently Amended) An apparatus for minimizing effects of ground noise on an input buffer receiver, said apparatus comprising:  
  
means for forming a buffer input portion for receiving an input signal on a substrate;

means for forming a bias node within said buffer input portion;

means for connecting said a lower supply voltage to said buffer input  
portion;

means for forming a large capacitor between the bias node and the lower  
supply voltage ~~said large capacitor~~ for providing a coupling ratio  
between said large capacitor and a parasitic capacitor coupled  
between said bias node and a ground reference point ~~approaching is~~  
approximately equal to a unity value such that a biasing voltage at said  
biasing node follows said lower supply voltage to minimize effects of  
[[a]] said ground noise signal ~~between the lower supply voltage and~~  
the ground reference point; and

means for forming a buffer output portion on said substrate in  
communication with the buffer input portion for producing an output  
signal.

34. (Currently Amended) The apparatus of ~~claim 23~~ claim 33, wherein forming  
the buffer input portion further comprises:

means for forming a first transistor of a first conductivity type on said  
substrate;

5 means for applying the lower supply voltage to a source node of the first  
6 transistor;

7 means for applying a reference voltage to a gate node of the first  
8 transistor;

9 means for connecting a drain node of the first transistor to develop as  
10 biasing voltage at said drain node;

11 means for forming a second transistor of a second conductivity type on  
12 said substrate;

13 means for connecting a drain node of the second transistor to the drain  
14 node of the first transistor;

15 means for connecting a gate node of the second transistor to the drain  
16 node of the first transistor for developing the biasing voltage; and

17 means for connecting a source node of the second transistor to an upper  
18 supply voltage;

19 means for forming a third transistor of the second conductivity type on said  
20 substrate;

21        ~~means for connecting a drain node of the third transistor to the drain of a~~  
22        ~~fourth transistor;~~

23        means for connecting a gate node of the third transistor to the drain node  
24        of the first transistor for developing the biasing voltage;

25        means for connecting a source node of the third transistor to the upper  
26        supply voltage source;

27        means for forming a fourth transistor of the first conductivity type on said  
28        substrate;

29        means for connecting a source node of the fourth transistor to the lower  
30        supply voltage;

31        means for connecting a gate node of the fourth transistor to receive **[[an]]**  
32        said input signal ~~externally~~; and

33        connecting a drain node of the fourth transistor to ~~an input to a drain node~~  
34        of the third transistor and to an input of the buffer output portion.

1    35.    (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein the first  
2        and fourth transistors are NMOS transistors, and the second and third  
3        transistors are PMOS transistors.



1 36. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means  
2 for forming the large capacitor comprises:

3 means for connecting said large capacitor between the sources of the first  
4 and fourth transistors of the buffer input portion and the gate of the  
5 second transistor of the buffer input portion.

1 37. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means  
2 for forming the buffer input portion further comprises:

3 means for connecting the gate of the second transistor to its drain.

1 38. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means  
2 for forming the buffer input portion further comprises the steps of:

3 means for connecting the gate of the second transistor to the gate of the  
4 third transistor.

1 39. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means  
2 for forming the buffer output portion which produces said output signal  
3 comprises:

4 means for forming a first inverter on said substrate; and

means for connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth ~~transistor~~; transistor.

40. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal to minimize the effects of ground noise on a delay jitter factor of said input buffer.

41. (Currently Amended) The apparatus of ~~claim 23~~ claim 33, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{C_p + CHC} \approx 1$$

where:

**CHC** is the capacitance value of the large capacitor

**CHC**, and

**C<sub>p</sub>** is the capacitance value of the parasitic capacitor

**C<sub>p</sub>**.

1    42.    (Currently Amended) The apparatus of ~~claim 23~~ claim 33, wherein the  
2           capacitance value of the large capacitor ~~relative to~~ is chosen to be very  
3           large with respect to a capacitance value of said parasitic capacitor and  
4           results in a quicker response time for the output signal.